IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus comprising:

a substrate;

a first device including a gate electrode on a surface of the substrate in an area of the substrate defined by a first well;

a single crystal silicon alloy material disposed in each of a first junction region and a second junction region in the substrate adjacent the gate electrode of the first device, wherein (a) a lattice spacing of the silicon alloy material is different than a lattice spacing of a material of the first well of the substrate and (b) a surface of the first junction region and a surface of the second junction region are in a non-planar relationship with the surface of the substrate;

a second device complementary to the first device and comprising junction regions defined by doped portions of a material of a second well of the substrate, the material of the second well having a conductivity type different than a conductivity type of the first well; and

an etch stop layer conformally disposed on the substrate on the second device exclusive of the first device, wherein the etch stop layer covers exposed surfaces of the second device and causes tensile stress in the second device.

2. (Original) The apparatus of claim 1, wherein a surface of the substrate defines a top surface of the substrate and the surface of the first junction region and the surface of the second junction region are superior to the top surface of the substrate.

3. (Original) The apparatus of claim 1, wherein the surface of the first junction region and the surface of the second junction region are superior to the top surface of the substrate by a length in the range of between 5 nanometers and 150 nanometers.

4. (Previously Presented) The apparatus of claim 3, wherein the first junction region and the second junction region define a depth in the range of between 30 nanometers and 250 nanometers in depth below the surface of the substrate.

5-6. (Canceled)

7. (Previously Presented) The apparatus of claim 1 , wherein the lattice spacing of the silicon alloy material is larger than the lattice spacing of the material of the first well of the substrate.

8. (Original) The apparatus of claim 1, wherein a surface of the substrate proximate to the first junction region defines a first substrate sidewall surface and a surface of the substrate proximate to the second junction region defines a second substrate sidewall surface and the silicon alloy material disposed in the first junction region is attached to the first substrate sidewall surface and the silicon alloy material disposed in the second junction region is attached to the second substrate sidewall surface.

9. (Canceled)

10. (Original) The apparatus of claim 1, wherein the silicon alloy material comprises one of silicon germanium ($Si_{y-x}Ge_x$), silicon carbide ($Si_{y-x}C_x$), nickel silicide (NiSi), titanium silicide ($TiSi_2$), and cobalt silicide ($CoSi_2$).

11. (Original) The apparatus of claim 1, further comprising a layer of silicide material on the surface of the first junction region, the surface of the second junction region, and the gate electrode, wherein the layer of silicide material comprises one of nickel silicide (NiSi), titanium silicide ($TiSi_2$), and cobalt silicide ($CoSi_2$).

12. (Original) The apparatus of claim 11, further comprising a layer of conformal etch stop material on the layer of silicide material, wherein the layer of etch stop material comprises one of silicon dioxide (SiO_2), phosphosilicate

glass (PSG, a Phosphorous doped SiO_2), silicon nitride (Si_3N_4), and silicon carbide (SiC).

13. (Original) The apparatus of claim 12, further comprising a layer of dielectric material comprising on the layer of conformal etch stop material, wherein the layer of dielectric material comprises one of carbon doped oxide (CDO), cubic boron nitride (CBN), silicon dioxide (SiO_2), phosphosilicate glass (PSG), silicon nitride (Si_3N_4), fluorinated silicate glass (FSG), and silicon carbide (SiC).

14. (Currently Amended) An apparatus comprising:

a substrate;

a first device including a gate electrode on a surface of the substrate and a first junction region and a second junction region in the substrate adjacent the gate electrode, the first junction region and the second junction region defining a channel in a first well of the substrate; and

a single crystal silicon alloy material disposed in each of the first junction region and the second junction region such that a surface of the first junction region and a surface of the second junction region are superior to the top surface of the substrate by a length sufficient to cause a strain in the first well of the substrate, wherein a lattice spacing of the silicon alloy material is different than a lattice spacing of a material of the well of the substrate;

a second device complementary to the first device and comprising a gate electrode on the surface of the substrate and junction regions defined by doped portions of a material of a second well of the substrate, wherein the material of the second well of a conductivity type different than a conductivity type of the first well; and

an etch stop layer conformally disposed on the substrate on the second device exclusive of the first device, wherein the etch stop layer covers exposed surfaces of the second device and causes tensile stress in the second device.

15. (Previously Presented) The apparatus of claim 14, wherein the first well of the substrate comprises an N-type material having an electrically

negative charge, and wherein the silicon alloy material comprises a P-type junction region material having an electrically positive charge.

16. (Original) The apparatus of claim 15, wherein the silicon alloy is silicon germanium having a lattice spacing that is larger than a lattice spacing of the N-type channel/well material, and wherein the strain is a compressive strain.

17-27. (Canceled)

28. (Previously Presented) The apparatus of claim 1, wherein the second device comprises a gate electrode on the surface of the substrate, the apparatus further comprising:

relative to an area defined by the first well and an area defined by the second well, an etch stop layer selectively disposed on the surface of the substrate in an area defined by the second well such that the gate electrode of the second device is disposed between the etch stop layer and the substrate.

29. (Previously Presented) The apparatus of claim 14, wherein the second device comprises a gate electrode on the surface of the substrate, the apparatus further comprising:

relative to an area defined by the first well and an area defined by the second well, an etch stop layer selectively disposed on the surface of the substrate in an area defined by the second well such that the gate electrode of the second device is disposed between the etch stop layer and the substrate.